Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A composite NMOS device having a source connection, a drain connection and a gate connection for conducting an operating current comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gates of the first and second NMOS devices being coupled together through a bias control, the bias control providing a different bias to the gates of the first and second NMOS devices.;

the gate of the first NMOS device being coupled to the gate connection, the drain of the second NMOS device being coupled to the drain connection and the source of the first transistor being coupled to the source connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor.

2. (Original) The composite NMOS device of claim 1 wherein the gates of the first and second NMOS devices are connected together, and wherein the threshold of the first NMOS device exceeds the gate – source voltage of the second NMOS device when conducting the operating current.

3. (Original) The composite NMOS device of claim 2 wherein the second NMOS device is a native device.

4. (Original) The composite NMOS device of claim 2 wherein the second NMOS device has a substantially zero threshold.

5. (Canceled)

6. (Currently Amended) The composite device of claim [[5]] 1 wherein the bias control provides biases on the gates of the first and second NMOS devices so that the bias on the gate of the second NMOS device minus the bias on the gate of the first NMOS device is a function of the gate source voltage of the second NMOS device to ~~compensates~~ compensate for variations in temperature and processing.

7. (Currently Amended) The composite NMOS device of claim [[5]] 1 wherein the bias control is coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled together.

8. (Original) A composite NMOS device having a source connection, a drain connection and a gate connection for conducting an operating current comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gate of the second NMOS device being coupled to the source of the first NMOS device;

the gate of the first NMOS device being coupled to the gate connection, the drain of the second NMOS device being coupled to the drain connection and the source of the first transistor coupled to the source connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor.

9. (Original) The composite NMOS device of claim 8 wherein the second NMOS device is a native device.

10. (Original) The composite NMOS device of claim 8 wherein the second NMOS device has a substantially zero threshold.

11. (Original) The composite NMOS device of claim 8 wherein the gate of the second NMOS device is coupled to the source of the first NMOS device through a bias control.

12. (Original) The composite NMOS device of claim 11 wherein the bias control compensates for variations in temperature and processing.

13. (Original) The composite NMOS device of claim 12 wherein the bias control is coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled.

14. (Original) A source follower for conducting an operating current, the source follower having a positive power supply connection, a circuit ground connection, a source follower input connection and a source follower output connection comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate; and

a current source;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gates of the first and second NMOS devices being coupled together;

the gate of the first NMOS device being coupled to the source follower input connection, the drain of the second NMOS device being coupled to the positive power supply connection and the source of the first transistor being coupled to the source follower output connection and through the current source to the circuit ground connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor.

15. (Original) The source follower of claim 14 wherein the gates of the first and second NMOS devices are connected, and wherein the threshold of the first NMOS device exceeds the gate – source voltage of the second NMOS device when conducting the operating current.

16. (Original) The source follower device of claim 15 wherein the second NMOS device is a native device.

17. (Original) The source follower device of claim 15 wherein the second NMOS device has a substantially zero threshold.

18. (Original) The source follower device of claim 14 wherein the gates of the first and second NMOS devices are coupled through a bias control.

19. (Currently Amended) The source follower of claim 18 wherein the bias control provides biases on the gates of the first and second NMOS devices so that the bias on the gate of the second NMOS device minus the bias on the gate of the first NMOS device is a function of the gate source voltage of the second NMOS device to ~~compensates~~ compensate for variations in temperature and processing.

20. (Original) The source follower of claim 18 wherein the bias control is coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled.

21. (Original) A source follower for conducting an operating current, the source follower having a positive power supply connection, a circuit ground connection, a source follower input connection and a source follower output connection comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate; and

a current source;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gate of the second NMOS device being coupled to the source of the first NMOS device;

the gate of the first NMOS device being coupled to the source follower input connection, the drain of the second NMOS device being coupled to the positive power supply connection and

the source of the first transistor being coupled to the source follower output connection and through the current source to the circuit ground connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor.

22. (Original) The source follower of claim 21 wherein the second NMOS device is a native device.

23. (Original) The source follower of claim 21 wherein the second NMOS device has a substantially zero threshold.

24. (Original) The source follower claim 21 wherein the gate of the second NMOS device is coupled to the source of the first NMOS device through a bias control.

25. (Original) The source follower of claim 24 wherein the bias control compensates for variations in temperature and processing.

26. (Original) The source follower of claim 25 wherein the bias control is coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled.

27. (New) A composite NMOS device having a source connection, a drain connection and a gate connection for conducting an operating current comprising:

first and second NMOS devices each having a source, a drain and a gate;

third and fourth NMOS devices each having a source, a drain and a gate;

the sources of the third and fourth NMOS devices being connected to the drains of the first and second NMOS devices, respectively;

the gates of the third and fourth NMOS devices being coupled together and to a bias voltage;

the gates of the first and second NMOS devices being coupled together and to the gate connection;

the drains of the third and fourth NMOS devices being coupled to the drain connection;

the source of the first devices being capacitively coupled to the gates of the third and fourth NMOS devices;

the source of the second NMOS device being coupled to the source connection;

the third and fourth NMOS devices having lower threshold voltages than the first and second NMOS devices.

28. (New) The composite NMOS device of claim 27 wherein the first and third NMOS devices are replica devices for the second and fourth NMOS devices, respectively.

29. (New) The composite NMOS device of claim 27 wherein the third and fourth NMOS devices are native devices.

30. (New) The composite NMOS device of claim 27 wherein the third and fourth NMOS devices have a substantially zero threshold.

31. (New) A composite NMOS device having a source connection, a drain connection and a gate connection for conducting an operating current comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gates of the first and second NMOS devices being coupled together through a bias control, the bias control;

the gate of the first NMOS device being coupled to the gate connection, the drain of the second NMOS device being coupled to the drain connection and the source of the first transistor being coupled to the source connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor;

the bias control is coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled together.

32. (New) A source follower for conducting an operating current, the source follower having a positive power supply connection, a circuit ground connection, a source follower input connection and a source follower output connection comprising:

a first NMOS device having a source, a drain and a gate;

a second NMOS device having a source, a drain and a gate; and

a current source;

the source of the second NMOS device being connected to the drain of the first NMOS device;

the gates of the first and second NMOS devices being coupled together through a bias control;

the gate of the first NMOS device being coupled to the source follower input connection, the drain of the second NMOS device being coupled to the positive power supply connection and the source of the first transistor being coupled to the source follower output connection and through the current source to the circuit ground connection;

the second NMOS device having a lower threshold voltage than the first NMOS transistor

the bias control being coupled to the gate of the second NMOS device through a resistor, and wherein the gates of the first and second NMOS devices are AC coupled.